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METHOD OF FORMING A BARRIER METAL IN A SEMICONDUCTOR DEVICE

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to a method of forming a barrier metal in a semiconductor device, and more particularly, to a method of forming a barrier metal in a semiconductor device capable of preventing introduction of a conductive material into a base layer by a subsequent process, by forming the barrier metal after pores existing on the surface of an interlayer insulating film being a porous film are buried.

Background of the Related Art

As the degree of integration in the semiconductor device is increased, the distance between the metal lines is narrowed. Accordingly, there is a problem that the speed of the device is reduced since the parasitic capacitance between the metal lines is increased. In order to solve this problem, it is required that copper (Cu), etc. having a low resistivity and a good electrical conductivity be used as a material of the metal line instead of aluminum or tungsten that has been currently used. A low dielectric constant film is needed to be used as the insulating film instead of the existing oxide film having a dielectric constant of 4.

The low dielectric constant film includes an organic polymer film, an inorganic SiOC film and a porous film having porosities therein. Of them, the organic polymer film and the inorganic SiOC film have a dielectric constant of about 2.7, which is relatively high among the low dielectric constant film.

The porous film can improve a low dielectric constant characteristic by controlling the ratio of the pore within the film. This porous material is made by a method by which air bubbles of a small size are formed within the film in the course of curing a precursor of a sol state or a weak coupling between TEOS particles being the precursor, and a solvent is abruptly volatilized to keep the porous structure intact. In this process, silica mesh count within the porous material and the pore structure are changed depending on a drying method of the solvent. If the solvent is volatilized by an annealing process like the curing of the SOG film, a material having a dense structure is formed while the porous material shrunk, so that it does not have a desired characteristic of the porous film having a low dielectric constant. Therefore, the porous material is formed by means of a supercritical drying method of abruptly volatilizing the solvent in a condition of over a triple point in the solvent. Another method includes making precocious the solvent as a special solvent at the normal pressure to form the porous material. As the pore has a dielectric constant of 1 in the air, it is required that the ratio of the pore be increased or the dielectric characteristic of silica be lowered in order to form a film of a low dielectric constant. In case of the former, however, if the ratio of the pore is increased, mechanical stability is lowered since a structural

strength of the film is weaken. For this reason, there is a problem that the low dielectric constant film could not hold the weight when a subsequent CMP process, etc. implemented.

A method of manufacturing the semiconductor device using the above porous film will be described by reference to FIG. 1A and FIG. 1B.

Referring to FIG. 1A, a first SiC layer **12**, a porous film **13** and a second SiC layer **14** are formed on a base layer **11**. A via hole **10** trough which a part of the base layer **11** is exposed is then formed by a patterning process. As described above, a plurality of pores **15** are formed in the porous film **13**. In particular, pores **16** are formed at the sidewalls of the via hole **10**.

By reference to FIG. 1B, a barrier metal **17** is formed on the entire structure including the via hole **10**. At this time, the barrier metal **17** is broken off due to the pores at the sidewalls of the via hole **10**, so that a broken-off region **18** is formed. In the porous film, the size of the pore is approximately 10~40Å and the density of the pore is about 30~50%. Copper is infiltrated into the base layer **11** due to discontinuity of this barrier metal when a subsequent seed metal, copper, etc. buried, which degrades the characteristic of the device.

SUMMARY OF THE INVENTION

Accordingly, the present invention is contrived to substantially obviate one or more problems due to limitations and disadvantages of the related art, and an object of the present invention is to provide a method of forming a barrier metal in a semiconductor device capable of preventing introduction of a

conductive material into a base layer in a subsequent process, by burying pores existing on the surface of an interlayer insulating film being a porous film and then forming the barrier metal.

Additional advantages, objects, and features of the invention will be set forth in part in the description which follows and in part will become apparent to those having ordinary skill in the art upon examination of the following or may be learned from practice of the invention. The objectives and other advantages of the invention may be realized and attained by the structure particularly pointed out in the written description and claims hereof as well as the appended drawings.

To achieve these objects and other advantages and in accordance with the purpose of the invention, as embodied and broadly described herein, a method of forming a barrier metal in a semiconductor device according to the present invention is characterized in that it comprises the steps of a) patterning a porous film on a base layer to form a via hole, b) depositing a CVD TiN film on the entire structure including the via hole, c) implementing a plasma treatment process using $N_2 + H_2$, d) repeatedly implementing the steps (b) and (c) in order to bury only the pores formed on the surface of the porous film with CVD TiN, and e) forming a barrier metal on the entire structure including the via hole.

In another aspect of the present invention, it is to be understood that both the foregoing general description and the following detailed description of the present invention are exemplary and explanatory and are intended to provide further explanation of the invention as claimed.

BRIEF DESCRIPTION OF THE DRAWINGS

The above and other objects, features and advantages of the present invention will be apparent from the following detailed description of the preferred embodiments of the invention in conjunction with the accompanying drawings, in which:

FIG. 1A and 1B are cross-sectional views of semiconductor device for explaining a conventional method of forming a barrier metal in the device; and

FIG. 2A through FIG. 2D are cross-sectional views of semiconductor device for explaining a method of forming a barrier metal in the device according to a preferred embodiment of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

Reference will now be made in detail to the preferred embodiments of the present invention, examples of which are illustrated in the accompanying drawings, in which like reference numerals are used to identify the same or similar parts.

FIG. 2A through FIG. 2D are cross-sectional views of semiconductor device for explaining a method of forming a barrier metal in the device according to a preferred embodiment of the present invention.

Referring to FIG. 2A, a first SiC layer **202**, a porous film **203** and a second SiC layer **204** are formed on a base layer **201**. A via hole **100** trough which a part of the base layer **201** is exposed is then formed by a patterning process. A plurality of pores **205** are formed in the porous film **203**. In

particular, pores **206** are formed at the sidewalls of the via hole **100**.

By reference to FIG. 2B, a CVD TiN film **200** is deposited in thickness of 10 ~ 20 Å on the entire structure including the via hole **100** using a TDMA source. At this time, the CVD TiN film has a very good step coverage and MOTiN being CVD TiN may be deposited.

Next, a plasma treatment process is implemented using $N_2 + H_2$ gas. C, O, S, etc. within the CVD TiN film **200** are coupled with hydrogen by this plasma treatment and are then pumped out. The thickness of the CVD TiN film 20 is also reduced. Accordingly, the pores on the surface of the porous film 3 is gradually buried with CVD TiN.

Deposition of CVD TiN and plasma treatment are repeatedly implemented so that only the pores are completely buried by adequately controlling the thickness of CVD TiN and a plasma treatment time, as shown FIG. 2C.

Turning to FIG. 2D, a barrier metal **210** and a seed metal **211** are deposited on the entire structure including the via hole **100**. A conductive material **212** such as copper (Cu) is then buried.

As the pores formed on the surface of the porous film are removed by the above process, a phenomenon that the conductive material is introduced into the underlying structure through the pores could be eliminated.

As described above, according to the present invention, after the pores existing on the surface of the interlayer insulating film being the porous film are buried, the barrier metal is formed. Therefore, the present invention has a new effect that it can prevent introduction of the conductive material into the

base layer in a subsequent process.

The forgoing embodiments are merely exemplary and are not to be construed as limiting the present invention. The present teachings can be readily applied to other types of apparatuses. The description of the present invention is intended to be illustrative, and not to limit the scope of the claims. Many alternatives, modifications, and variations will be apparent to those skilled in the art.